How to use the Timing System as a Client

April 6, 2012

Controls Software
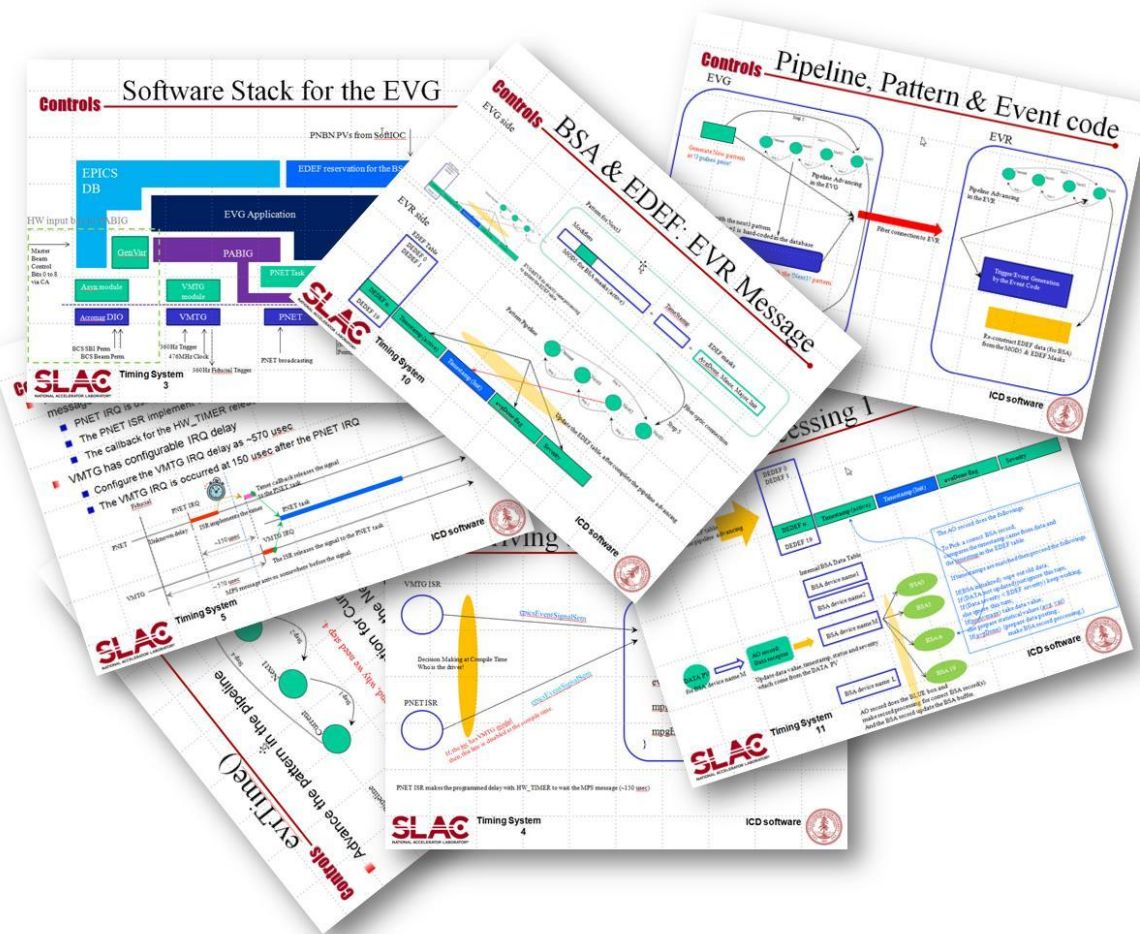
Contents

Controls

- EVR Low Level Screens

- How to make triggers with the Low Level Screens

- What is the relationship between Low Level Screen and High Level Screen

- How to set up the EVR in your application

- Form factor & OS dependency on the EVR : go to first place with photo

- What is BSA

- How does BSA work

- How to Setup BSA

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Complicated…

Controls

EVR Diag. Screen

(D1) Board information

(D2) Board Control and Monitoring

(D4) Extended Delay Front Panel Trigger

(D3) Trigger Selection Key for Front Panel

(D5) Regular Trigger Control

(D6) VME IRQ delay configuration
Don't Use It!

Cont'd: EVR Diags

- **EVR Board**
    - Board Type/Instance/IRQLevel/FPGA version (see D1)
    - Board Enable/Disable (see D2)
    - RX link Status (D2)
    - Error Counter and Reset (D2)

- **Extended Trigger/Front Panel Trigger** (D3/D4)

- **Rear Panel Trigger** (D5)

- **VME delayed IRQ (Not Use)** (D6)

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Ext. Delay Trigger?/Front Panel Trigger?

- **Front Panel Trigger**
  - Physically located on the front panel (D4)
    - VME: 4 Channels
    - PMC: 3 Channels
  - Select the Real Trigger Channel and route to Front Panel
    - Configure with the trigger selection key from 11 to 24 (please, see the trigger selection key list in the D3 session)
    - Uses same delay and width as the rear trigger which is selected by the trigger selection key

- **Extended Delay Trigger**
  - Physically using same output channel with the front panel trigger
  - Shares same event code with the rear transition
  - Configure with the trigger selection key from 0 to 3 (please, see the trigger selection key list in the session D3)
  - Has its own delay, width and prescaler

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Extended Delay and Prescaler

- Max Width: 64k (16 bits)

- Max Delay: 4.3E+9 (32 bits)

- Need more longer delay? Then the Extendeded Delay
  - Extended Delay = Delay x Prescaler (32 bits)
  - Thus, we have 64 bits wide delay counter for the extended delay

- PMC EVR has only 2 prescalers for the first 2 channels

- Thus, the third channel on the front panel
  - is NOT available as the Extended Trigger
  - is available as the Front Panel Trigger

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Trigger Panel

Controls

(T1) event code for trigger generator

(T2) enable/disable the event code (only for the trigger generator)

(T3) matrix switches for mapping the events to the trigger channel

How to control the trigger

Controls

Triggers Panel PVs

Event Code PV

(T1)

Enable/Disable PV

(T2)

Triggers Panel PVs

Matrix switches on the trigger panel

(T3)

Trigger Event

Prescaler PV

Delay PV

Width PV

EVR Diag. Panel PVs (D4 and D5)

Status PV

Polarity PV

An Internal Clock

Prescaler

Delay Counter

Width Counter

Trigger Generator

set

clear

Enable/Disable

Trigger Driver

Polarity control

Hardware Channel

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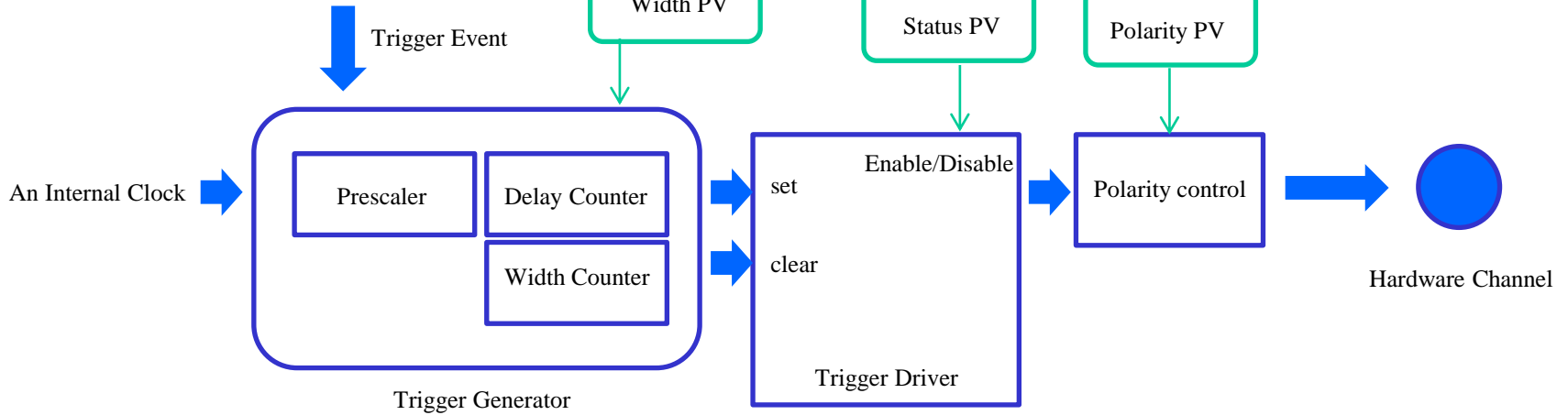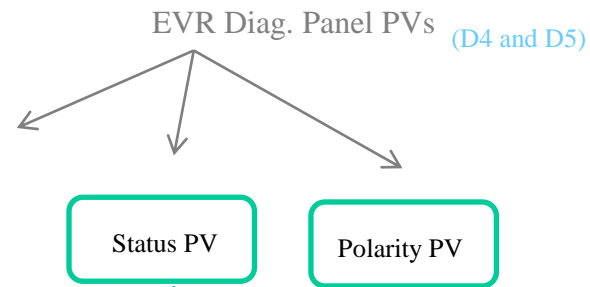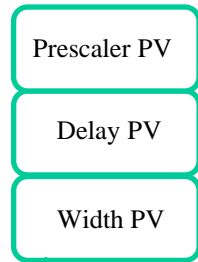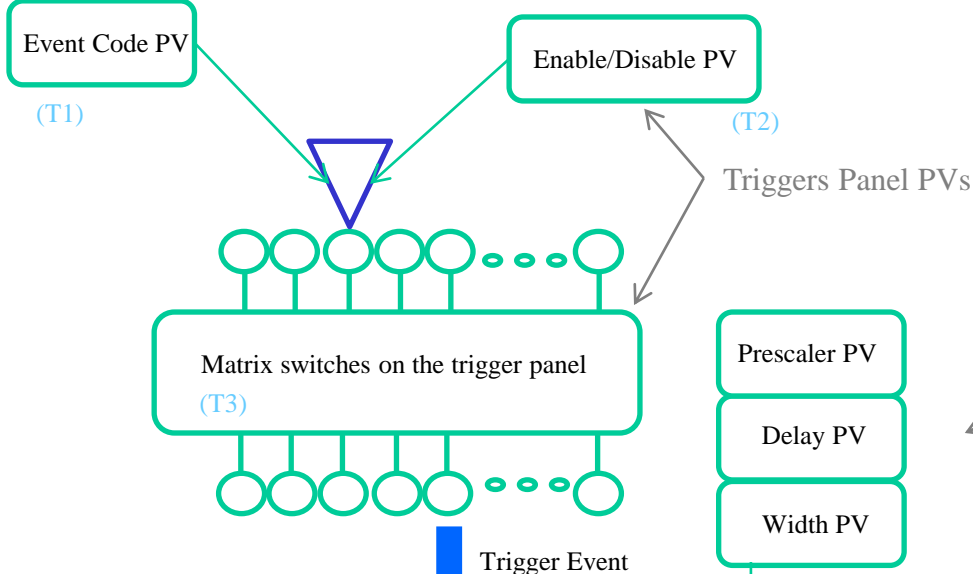
Form Factor/OS dependency

Controls

Event Module for RTEMS/vxWorks

- EVR Processing Logic
  - erRecord
  - devErMrf
  - drvErMrf
  - mrfCommon/mrfVme64
- BSA

- VME EVR Hardware
- PMC EVR Hardware
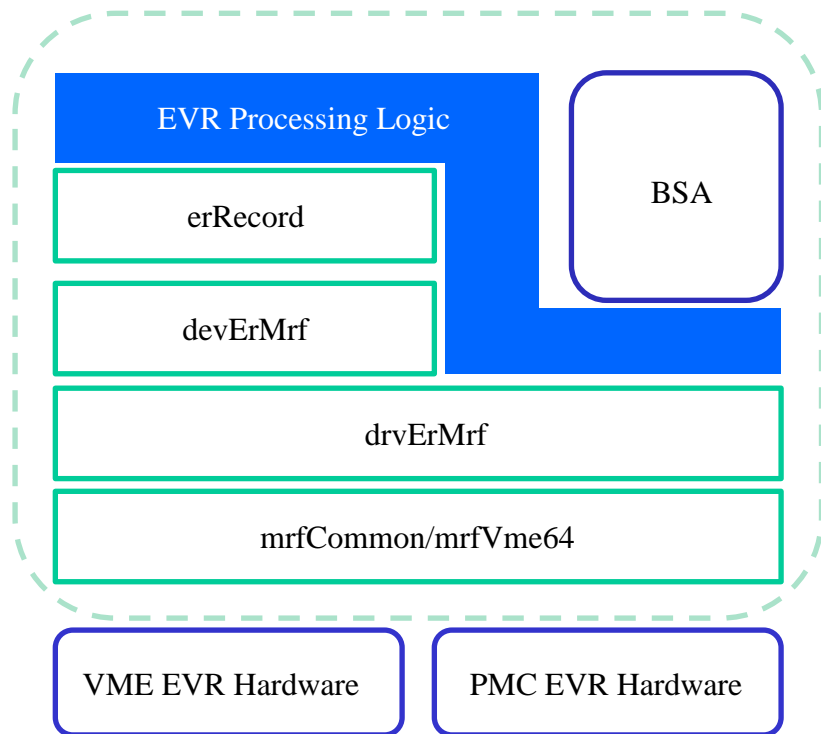
Works with old register map

Event Module for Linux

- EVR Processing Logic
  - erRecord
  - devErMrf
  - drvLinuxEvr
  - erapi
- BSA

- PMC EVR Hardware
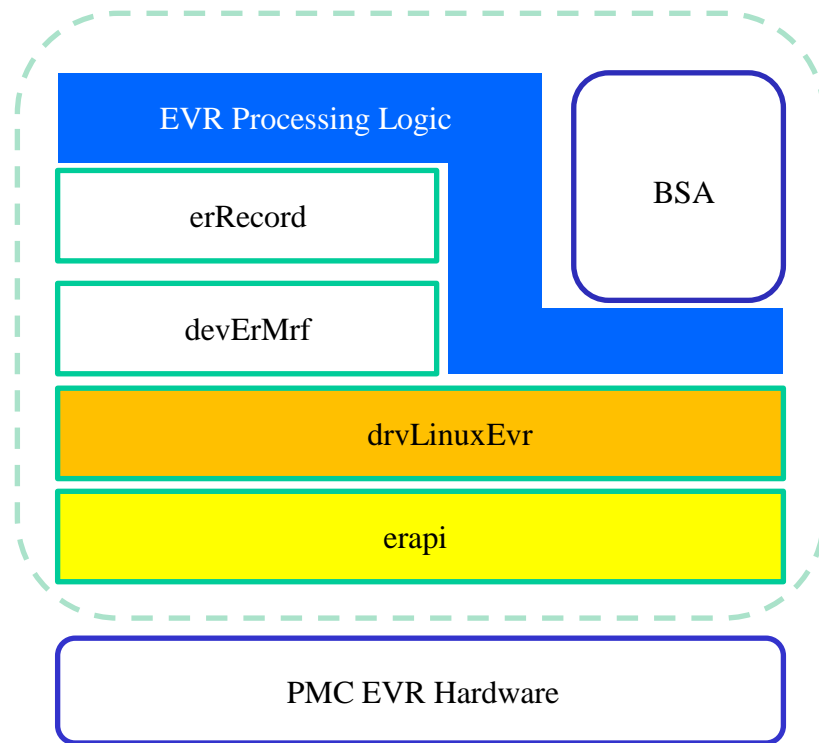
Works with modular register map (new)

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High Level Screen

Issue 1: FWD/BWD Propagation

Low Level PVs
on Diagnostics Screen

High level PVs
on Events Screen

Event
Number[3*]

Event Number
on Trigger Screen

Forward/Backward Propagations [*]

Save/Restore for High Level PVs [*]

Hard-coded Event number
and Trigger Configuration[2*]

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Issue 2: Event Code Invariant Delay

- Each Event Code has its own offset
    - Each event code has to have different offset
    - The delay has been hard-coded in the EVG
    - EVG assumes there is no duplicated offset

Event information in EVG

- These offsets are involved in the hardware trigger calculations for

  trigger delay on EVR side

    - But, the offset PV is hard-coded for each trigger channel
    - Thus, the changing event code (or, changing trigger selection) makes different delay
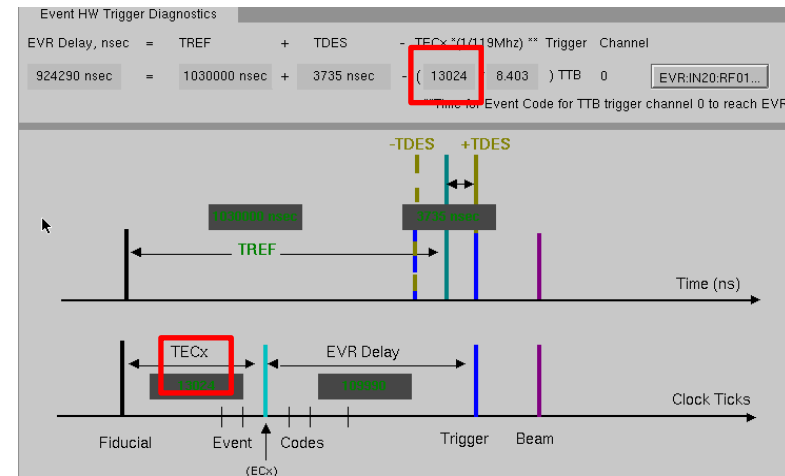
Trigger Delay Calculation in the EVR

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Event Code and Delay

- Delay Calculation

Clock Rate

$$T_{delay} = T_{ref} + T_{des} - \{T_{ec} \cdot (1/119MHz)\}$$

Fiducial to Beam: Constant

Desired Delay

Event Code Offset by EVG

- To make "event code invariant delay", need to fix the hard-coded part
  - Require to detect changing event code (or, changing trigger selection)
  - Re-calculate the forward propagation
  - Actually, the offset of event code is a function of event code and trigger configuration

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Event Module

- Pick a correct event module
  - R3-14-8-2
    - Please, use event-R3-3-1
    - for LCLS, FACET
    - back-propagation, event invariant delay
    - requires the standalone generaltime package
  - R3-14-12
    - Please use event-R3-2-2-br_generaltime-2-1
    - for LCLS, FACET and XTA
    - bundled generaltime in EPICS base
    - back-propagation, event invariant delay
    - mrfApi for linux platform
    - Info(autosaveFields_pass0, "VAL") + PINI=YES in evrDevTrig.db
    - Additional macros to bsaTOROEdef.substitutions, egu, hopr, lopr, prec, adel
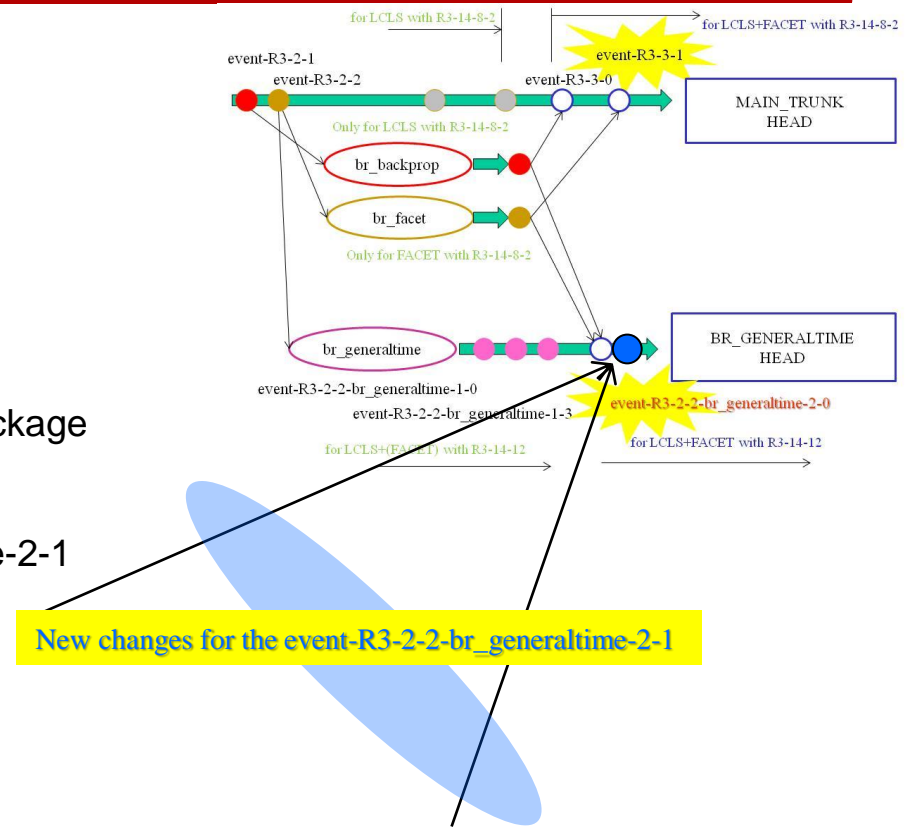
Notice) The latest update (to fix bugs for the Linux PMC EVR) is still stuck in the HEAD of the branch for the R3-14-12. Thus, there will be another release very soon!

*evr.substitutions

- EVR record instance + EVR event instances
  - EVR record instance / need to choose one of the followings
    - evr.db
      - Simplest one
      - DEV, CARD, DELAY, WIDTH
    - evrWithDelays.db
      - More degree of freedom for delays
      - DEV, CARD, DELAY[0_9, A_D], WIDTH
    - evrWithExtDelays.db
      - evr.db + more degree of freedom for front panel trigger channels
      - State, Width, Delay, Prescaler, Polarity for each front panel channels
    - evrWithFrontPanel.db
      - Similar with evrWithFronPanel
      - Disable Rear panel trigger
      - Less degree of freedom: DEV, CARD, WIDTH DELAY

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Cont'd : EVR Instance

EVR record instance and the EVR Diag Screen

Cont'd

- **EVR event instances**
  - controls the mapping between event code and trigger channel
  - Use evrEventCtrl.db
  - DEV, CARD, NAME, ID, P0-P13, VME
    - NAME: EVENT1 to EVENT14
    - ID: Event code
    - Pn: 0 to 1 for the matrix switch
    - VME: Enable the softevent

P0 to P13

VME

ID: Event code

Hard-coded

Example of *evr.substitutions

Controls


```
file evrWithDelays.db
{
#                      Pulse
#      Device    Card  Width  Channel Delays (clock ticks)
pattern { DEV        , CARD , WIDTH , DELAY0, DELAY1, DELAY2, DELAY3, DELAY4, DELAY5, DELAY6, DELAY7, DELAY8, DELAY9, DELAYA, DELAYB, DELAYC, DELAYD }
        { EVR:LI24:RF01,  0  ,  12   , 110000, 110000, 110000, 110000, 110000, 110000, 110000, 110000, 110700, 110000, 110000, 110000, 110000, 110000 }
}
file evrEventCtrl.db
{
#      Device      Card  <--------------------------  Event  -------------------------->
pattern { DEV          , CARD , NAME    , ID ,P0,P1,P2,P3,P4,P5,P6,P7,P8,P9,P10,P11,P12,P13,VME}
        { EVR:LI24:RF01,  0  , EVENT1  , 40 , 0, 1, 0, 1, 0, 1, 0, 1, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT2  , 41 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT3  , 42 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 1 , 1 , 1 , 0 }
        { EVR:LI24:RF01,  0  , EVENT4  , 43 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT5  ,140 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT6  ,141 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT7  ,142 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT8  ,143 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT9  ,151 , 1, 0, 1, 0, 1, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT10 ,152 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT11 ,154 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT12 ,155 , 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT13 ,156 , 0, 0, 0, 0, 0, 0, 1, 0, 0, 0 , 0 , 0 , 0 , 0 }
        { EVR:LI24:RF01,  0  , EVENT14 ,157 , 0, 0, 0, 0, 0, 0, 0, 0, 1, 0 , 0 , 0 , 0 , 0 }
}
```

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*pattern.substitutions

- First Session for evrPattern.db
  - Records for the pipeline related PVs
  - Just use evrPatternAll.db
  - Need to specify ACTIVE TIMESLOT
    - LCLS: 1 and 4
    - FACET: 2 and 5
    - XTA: 3 and 6
- Second Session for Events
  - for the Event records
  - Each beam program has different event sets
  - Need to use a proper template
    - LCLS: evrEventAll.db
    - FACET: evrEventFACET.db
    - XTA: evrEventXTA.db

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Example of *pattern.substitutions

Specify proper ACTIVE TIMESLOT for each beam program

```
file evrPatternAll.db
{
#         Device          ,  SLC Pattern, EVR/Trigger
#                                          Links
  pattern { DEVICE         ,  LINK4       , LINK5 , LINK6 , TREF    , TS1ST , TS2ND }
# 7/3/8: TS1ST=0 for 16.6 ms valid flag; 1 for 8.3 ms
          { IOC:IN20:RF01 ,  ""          , ""    , ""     , 1.03E06 ,  1  ,   4   }
}
file evrEventAll.db
{
  pattern { DEVICE         }
          { IOC:IN20:RF01 }
}
```

Choose a proper template for the each beam program

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What is the Timeslot

- Zero Crossings at AC 3 phases lead out the 6 time slots

- Same Timeslot in different peroid shows exactly same AC phase configuration.

- Active Timeslot
  - LCLS: TS1 and TS4
  - FACET: TS2 and TS5
  - XTA: TS3 and TS6

- Primary Timeslot
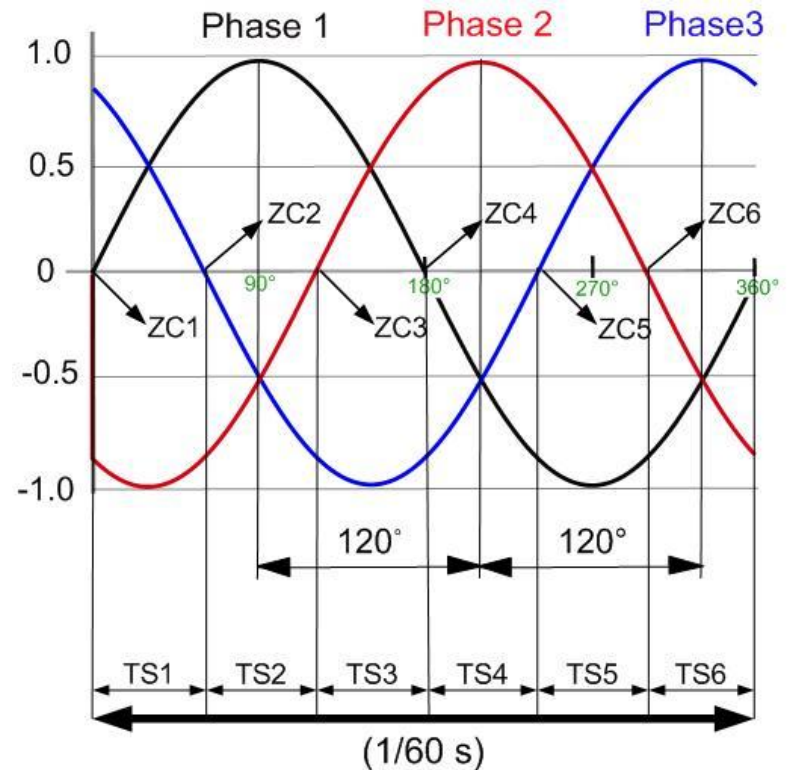
ZC = Zero Crossing
TS = Time Slot

Controls *trig.substitutions

- Make PV for the High Level Screen

- Use, evrDevTrig.db

- Add 2 new macros for new features

  - Backward Propagation

  - Event Code Invariant Delay

  - TOUT

    - Make mapping between logic and output channel

    - OUT0 to OUT9 and OUTA to OUTD

    - For the front panel re-use OUT0 to OUT3

  - ACTV

    - Enable/Disable the event code invariant delay

- Timing Usability project to auto-generate trigger EDM screens

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Example of *trig.substitutions

For trigger screen autogeneration:
1) Add comment tags & 2) modify Makefile (next slide)

New macros

Optional tags for LCLS; necessary for other facilities

```
file evrDevTrig.db
{
#          Device        , Description      ,polarity,width,delay,event , EVR  , EVR,  IOC
#                                                    code  ,location,unit
  pattern { DEV          ,  DESC            ,POL, WID, DES , TEC        , LOCA , UNIT, IOC          , DRVL , DRVH , TCTL , TPOL, TWID, TDES, CTL, TOUT, ACTV}
#EVR EVR:LI24:RF01             #CONTROLPV1 SIOC:SYS0:AL00:MODE
#FILE evnt_li24_llrf           #CONTROLPV2 SIOC:SYS0:AL00:TOD
{ ACCL:LI24:100:KLY_C_1_ ,  "24-1 PAC Acc" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP0 , OT0P, OT0W, OT0D, 1,   OUT0, 1 }
{ ACCL:LI24:100:KLY_C_2_ ,  "24-1 PAC SB"  , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP1 , OT1P, OT1W, OT1D, 1,   OUT1, 1 }
{ ACCL:LI24:200:KLY_C_1_ ,  "24-2 PAC Acc" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP2 , OT2P, OT2W, OT2D, 1,   OUT2, 1 }
{ ACCL:LI24:200:KLY_C_2_ ,  "24-2 PAC SB"  , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP3 , OT3P, OT3W, OT3D, 1,   OUT3, 1 }
{ ACCL:LI24:300:KLY_C_1_ ,  "24-3 PAC Acc" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP4 , OT4P, OT4W, OT4D, 1,   OUT4, 1 }
{ ACCL:LI24:300:KLY_C_2_ ,  "24-3 PAC SB"  , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP5 , OT5P, OT5W, OT5D, 1,   OUT5, 1 }
{ TCAV:LI24:800:TC3_C_1_ ,  "L3TcavPAC(24-8)Acc",0 , 100,-31605, LCLSTCAV , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP6 , OT6P, OT6W, OT6D, 1,   OUT6, 1 }
{ TCAV:LI24:800:TC3_C_2_ ,  "L3TcavPAC(24-8)SB", 0 , 100, 3820 , TS4_30_  , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP7 , OT7P, OT7W, OT7D, 1,   OUT7, 1 }
{ TCAV:LI24:800:TC3_D_   ,  "L3TcavPAD(24-8)"  , 0 , 100, 3820 , LCRFONLY , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP8 , OT8P, OT8W, OT8D, 1,   OUT8, 1 }
{ LLRF:LI24:0:REF_C_     ,  "24-8KlyPAD/L3Pcav" , 0 , 100, 3820 , TS4_30_  , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTP9 , OT9P, OT9W, OT9D, 1,   OUT9, 1 }
# spare triggers 5-8 TTB 11-13
{ TRIG:LI24:RF05:        ,  "Spare Trig 5" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTPA , OTAP, OTAW, OTAD, 1,   OUTA, 1 }
{ TRIG:LI24:RF06:        ,  "Spare Trig 6" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTPB , OTBP, OTBW, OTBD, 1,   OUTB, 1 }
{ TRIG:LI24:RF07:        ,  "Spare Trig 7" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTPC , OTCP, OTCW, OTCD, 1,   OUTC, 1 }
{ TRIG:LI24:RF08:        ,  "Spare Trig 8" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTPD , OTDP, OTDW, OTDD, 1,   OUTD, 1 }

#{ ACCL:LI24:800:KLY_D_   ,  "24-8 Kly PAD" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , OTPE , OTEP, OTEW, OTED, 1,   NONE, 0 }

#  spare triggers 1- 4 FP (VME)
{ TRIG:LI24:RF01:        ,  "Spare Trig 1" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , DG0E , DG0P, DG0W, DG0D, 1,   OUT0, 1 }
{ TRIG:LI24:RF02:        ,  "Spare Trig 2" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , DG1E , DG1P, DG1W, DG1D, 1,   OUT1, 1 }
{ TRIG:LI24:RF03:        ,  "Spare Trig 3" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , DG2E , DG2P, DG2W, DG2D, 1,   OUT2, 1 }
{ TRIG:LI24:RF04:        ,  "Spare Trig 4" , 0 , 100, 3820 , TS4_30_   , LI24 , RF01, IOC:LI24:RF01, -2.8E06, 2.8E06 , DG3E , DG3P, DG3W, DG3D, 1,   OUT3, 1 }
}
```

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Example of xApp/Db Makefile

TOP=../../..

include $(TOP)/configure/CONFIG

 <snip>

Create and install (or just install) into <top>/db # databases, templates, substitutions like this

DB += IOC-XT01-IM01-adc.db

DB += IOC-XT01-IM01evr.db

DB += IOC-XT01-IM01pattern.db

DB += IOC-XT01-IM01bsa.db

DB += IOC-XT01-IM01trig.db

gen_trig_edl:

　　　create_edm_event_msi.py IOC-XT01-IM01trig.substitutions

 include $(TOP)/configure/RULES

#--------------------------------------

ADD RULES AFTER THIS LINE

****

New target
- Pass in *trig.substitutions file
  - For multiple EVRs, one file contains substitutions for every EVR, separated with appropriate #EVR, #FILE tags
  - edl trigger files specified by #FILE are output to $EDM/install directory

- Infrastructure will be ready for engineers to build after next week PAMM (4/10)

Bean Synchronous Acquisition (BSA)

- Acquire beam dependent scalar values across multiple IOCs to analyze the correlations among the values which are acquired at the same pulse

- Maintain the buffer up to 2800 points

- The buffered values can be averaged up to 1000 samples

- Up to 20 different BSA requests are available

- Each BSA requests can specify:

  - Beam Code

  - Inclusion/Exclusion Masks for the Event Pattern

  - Measurement Count (number of data points)

  - Average per Measurement

  - Severity Level

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How to Setup the BSA request EVG side

- Bring up the Event Global

- Choose Event Definition

- Make EDEF reservation with your own name

- Bring up your EDEF slot

- Set up Masks / Beam Code / Measurements/ Average/Severity

- Turn ON to start BSA

- Finally release your EDEF slot

Bring up the EDEF screeen

Controls

Event Global Screen

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Make EDEF Reservation

Controls

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Play with your EDEF slot

EDEF Slot

Mask Setup

Controls

EVG

EVR

Step 5

Current Next1 Next2 Next3

Step 4
Step 1 Step 2 Step 3

Generate New pattern
at !3 pulses prior!

Pipeline Advancing
in the EVG

Dealing with the next1 pattern
Pipeline index =1 is hard-coded in the database

Decide event code list with the !Next1! pattern

Construct EDEF data (for BSA) from the
MOD5 & EDEF Masks

Fiber connection to EVR

Step 4
Current Next1 Next2 Next3
Step 1 Step 2 Step 3

Pipeline Advancing
in the EVR

Trigger/Event Generation
by the Event Code

Re-construct EDEF data (for BSA)
from the MOD5 & EDEF Masks

BSA & EDEF: EVR Message

EVG side

Pattern for Next3

Modifiers		TimeStamp		EDEF masks
	+		+	AvgDone, Minor, Major, Init

MOD5 for BSA masks (active)

EDEF Table
DEDEF 0
DEDEF 1

Pattern Pipeline · Current · Next1 · Next2 · Next3
Step 4 · Step 1 · Step 2 · Step 3

DEDEF n · Timestamp (active) · Timestamp (Init) · avgDone flag · Severity
DEDEF 19
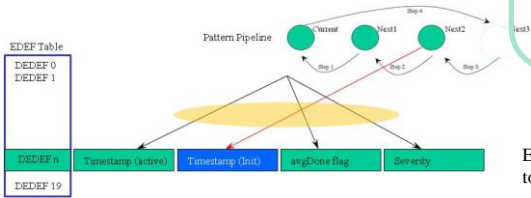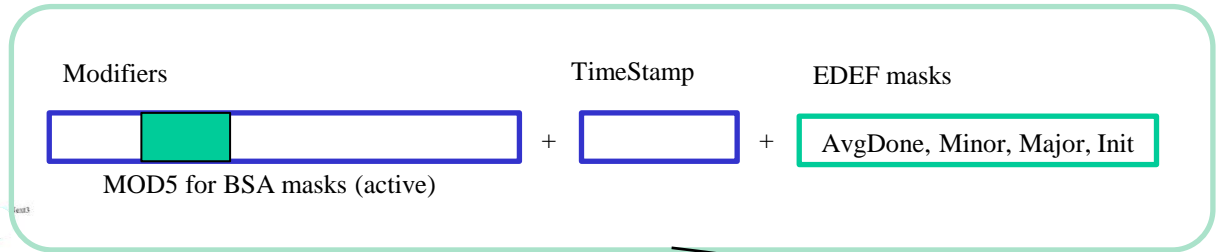
EVG&EVR do exactly same processing
to update the EDEF table

Fiber optic connection

Step 5

EVR side

Pattern Pipeline

Step 4

Current   Next1   Next2   Next3

Step 1   Step 2   Step 3

EDEF Table

DEDEF 0
DEDEF 1
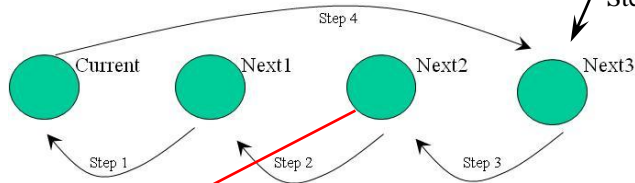
Update the EDEF table, after complete the pipeline advancing

DEDEF n	Timestamp (active)	Timestamp (Init)	avgDone flag	Severity

DEDEF 19

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BSA processing

Update EDEF table
After the pipeline advancing

DEDEF 0				
DEDEF 1				
DEDEF n	Timestamp (active)	Timestamp (Init)	avgDone flag	Severity
DEDEF 19				

Internal BSA Data Table

| BSA device name1 |
| BSA device name2 |
| BSA device name M |
| BSA device name L |

DATA PV
for BSA device name M

AO record:
Data receptor

BSA0

BSA1

BSA n

BSA 19

Update data value, timestamp, status and severity
which come from the DATA PV

AO record does the BLUE box and
make record processing for correct BSA record(s).
And the BSA record update the BSA buffer.

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How to setup the BSA in your application

Data Source

DATA source PV

DOL link:
  to get data and times stamp
  from Data source

FLNK

BSA

AO record

OUT link: (INST type)
  Specify secnName
  to make connection with data block

BSA record

INP (INST type)

IOSCAN request
to make record processing

History Buffers

Compression record: for vlaue

Compression record: for average

Compression record: for rms

BSA Device Support

API Calling

EVR Device Support
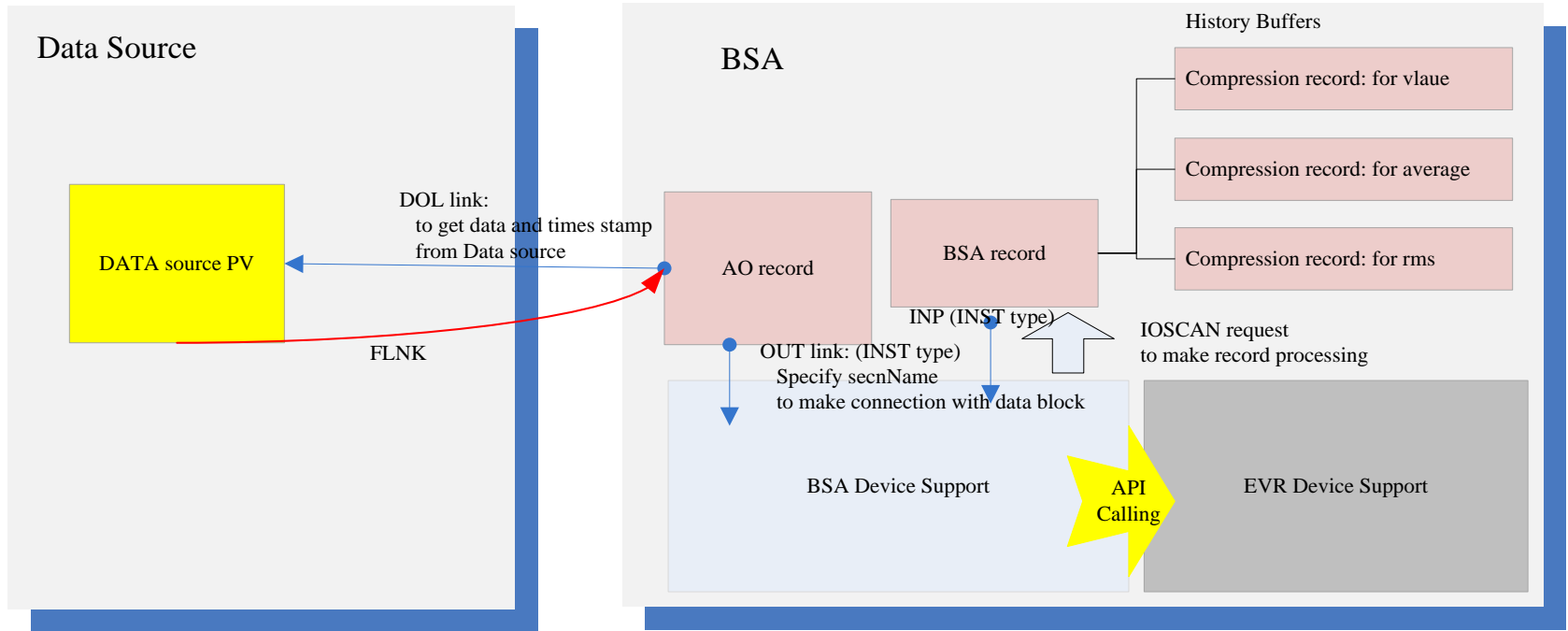
Your Application

BSA Package in Event Module

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- Pick a proper template: <…>Edef.db

- Example

Session for LLRF Phase

```
file bsaPHASEdef.db
{
#           Device              ,loc'n , IOC  , Attribute
  pattern {DEVICE              , LOC  ,  UN  , ATRB   , IN                    , SLCLNK}
          { TCAV:LI24:800       , LI24 , RF01 , P      , TCAV:LI24:800:TC3_PAVG, ""     }
# Future. To standardize for SCORE
#         { TCAV:LI24:800       , LI24 , RF01 , P      , TCAV:LI24:800:P       , ""     }
          { PCAV:LI25:300       , LI24 , RF01 , P      , PCAV:LI25:300:PH3_3_PACT, ""   }
# Future. To standardize for SCORE
#         { PCAV:LI25:300       , LI24 , RF01 , P      , PCAV:LI25:300:P       , ""     }
          { PCAV:LI29:100       , LI24 , RF01 , P      , PCAV:LI29:100:PH4_3_PACT, ""   }
# Future. To standardize for SCORE
#         { PCAV:LI29:100       , LI24 , RF01 , P      , PCAV:LI29:100:P       , ""     }
}
file bsaAMPLEdef.db
{
#           Device              ,loc'n , IOC  , Attribute
  pattern {DEVICE              , LOC  ,  UN  , ATRB   , IN                    , SLCLNK}
          { TCAV:LI24:800       , LI24 , RF01 , A      , TCAV:LI24:800:TC3_AAVG, ""     }
# Future. To standardize for SCORE
#         { TCAV:LI24:800       , LI24 , RF01 , A      , TCAV:LI24:800:A       , ""     }
          { PCAV:LI25:300       , LI24 , RF01 , A      , PCAV:LI25:300:PH3_3_AACT, ""   }
# Future. To standardize for SCORE
#         { PCAV:LI25:300       , LI24 , RF01 , A      , PCAV:LI25:300:A       , ""     }
# Future. To standardize for SCORE
#         { PCAV:LI29:100       , LI24 , RF01 , A      , PCAV:LI29:100:A       , ""     }
          { PCAV:LI29:100       , LI24 , RF01 , A      , PCAV:LI29:100:PH4_3_AACT, ""   }
}
```

Session for LLRF Amplitude

BSA device name   Location   Unit   Attribute   Data PV name

Timing system

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BSA templates

Template	Description	BSA properties
bsaAMPLEdef.db	RF Amplitude	Amplitude
bsaPHASEdef.db	RF Phase	Phase
bsaBLENEdef.db	Bunch Length	RAW, IMAX
bsaBLENTest.db	Fake for Test	
bsaBPMSCavityEdef.db	Cavity BPMs	Re(Hor), Im(Hor), Re(Ver), Im(Ver), RAW ref
bsaBPMSEdef.db	BPMs (stripline?)	X, Y, TMIT
bsaBPMSTest.db	Fake for Test	
bsaEnergyEdef.db	Beam Energy	Single Attribute
bsaFARCEdef.db	Faraday Cup/Bunch Charge	Charge
bsaFARCTest.db	Fake for Test	
bsaPMTEdef.db	PMT	QADC Raw
bsaPMTTest.db	Fake for Test	
bsaPWREdef.db	Beam Power	Power
bsaTOROEdef.db	Toroids/Beam current	TIMIT
bsaTOROTest.db	Fake for Test	
bsaWIREEdef.db	Wire Scanner	Position, Mask
bsaWIRETest.db	Fake for Test	

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BSA Check Point

- DOL field in data receptor
  - AO record in BSA facility
  - The data receptor gets data, timestamp, and severity from the DOL LINK.
  - DOL should be pointed your data source
- Data Source PV
  - Timestamp (BSA aware)
  - FLNK to the data receptor

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BSA aware Timestamp

- Basically, BSA facility compares the timestamp from data source and BSA event definition

- Assume, the timestamp from data source reflects ACTIVE_TIMESLOT and Pulse ID
  - ACTIVE_TIMESLOT: TS1 and TS4, event#0 in LCLS Event system
  - Pulse ID: lower 17 bits in nano-sec in timestamp

- TSE=-2 for your data source PV
  - if, our device support for data source PV, takes care the timestamp
  - Somewhere in device support should call the following function evrTimeGet(&pMyRec->timestamp, 0)

- TSE=0, -1 for your data source PV
  - If we can guarantee that record processing must be finished within 8.33 msec (time interval between active timeslot 1/120).

- TSE>1 for your data source PV
  - If we can not guarantee, the record processing can be finished within 8.33 msec (time interval between active time slot 1/120)
  - Or, data gettering is not synchronized with beam or event system.

BSA aware timestamp and BSA Success/Fail scenario (1)

Controls

Timestamps for active time slot

TSn   TSn+1

8.3 msec interval

Active Time Slot

Event for BSA concerned

Time

Get timestamp at this point

Device support processing

Record support processing

Undefined delay between Dev. and Rec.
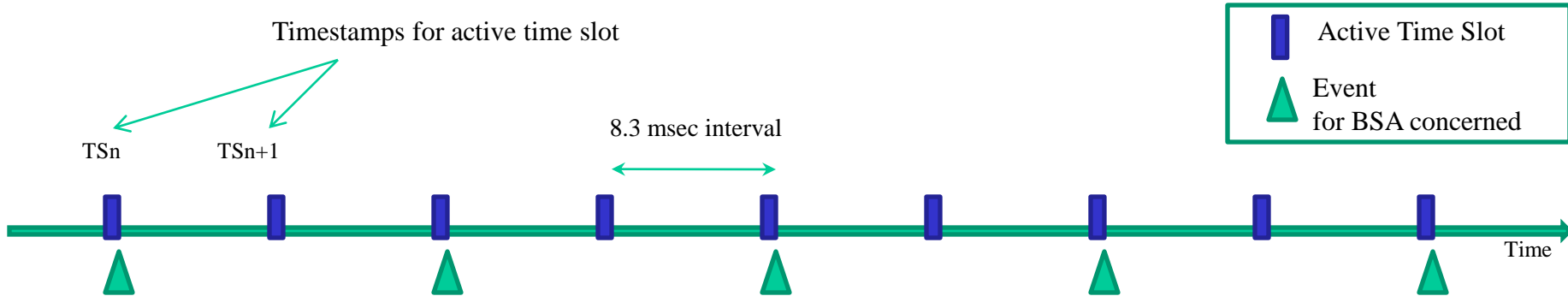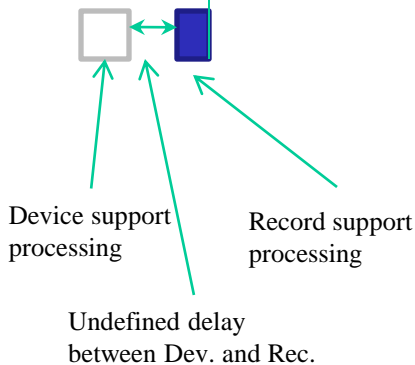
■ Success Scenario: if TSE=(0,-1) and Guaranteed everything can be finished before next active time slot (within 8.3 msec)

  ■ Device support gets data for TSn

  ■ When the record instance gets timestamp, it should be still TSn

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BSA aware timestamp and BSA fail/success scenario (2)

Timestamps for active time slot

TSn   TSn+1

8.3 msec interval

Active Time Slot

Event for BSA concerned

Time

Get timestamp at this point

Device support processing

Record support processing

Undefined delay between Dev. and Rec.
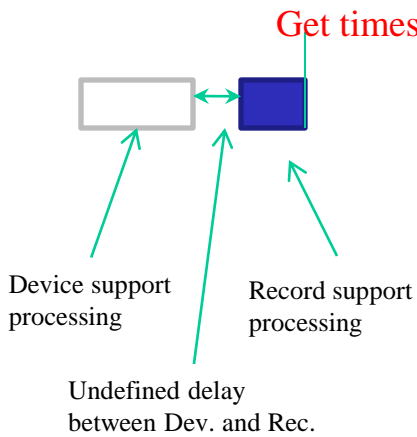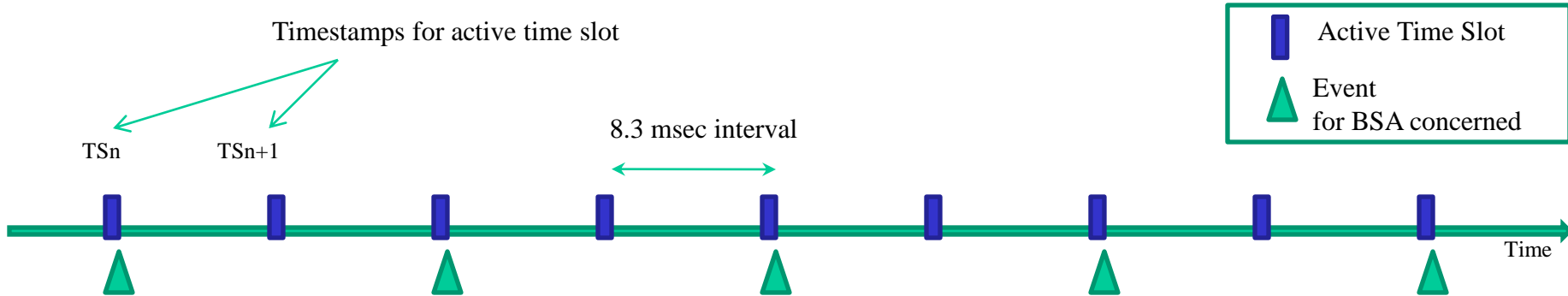
■ Fail Scenario: if TSE=0, -1

- ■ Device support successfully get data for TSn
- ■ But, need to assume, there should be undefined delay before start record processing
- ■ And, record processing might be not finished until next active timeslot
- ■ The record (the data source PV) time stamp gets TSn+1
- ■ Then, BSA could be failed.
  BSA assumed TSn timestamp for the data source PV

Timing system
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BSA aware timestamp
and BSA fail/success scenario (3)

Timestamps for active time slot

TSn   TSn+1

8.3 msec interval

Active Time Slot

Event
for BSA concerned

Time

Device support gets timestamp TSn
then, provides it to record

Device support
processing

Record support
processing

Undefined delay
between Dev. and Rec.
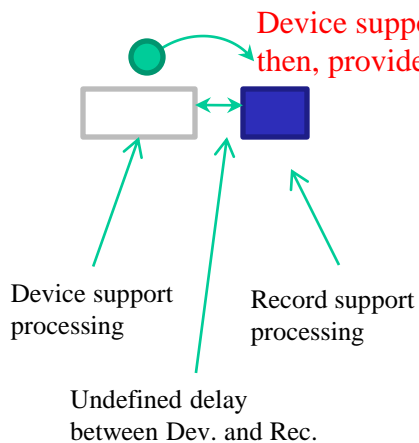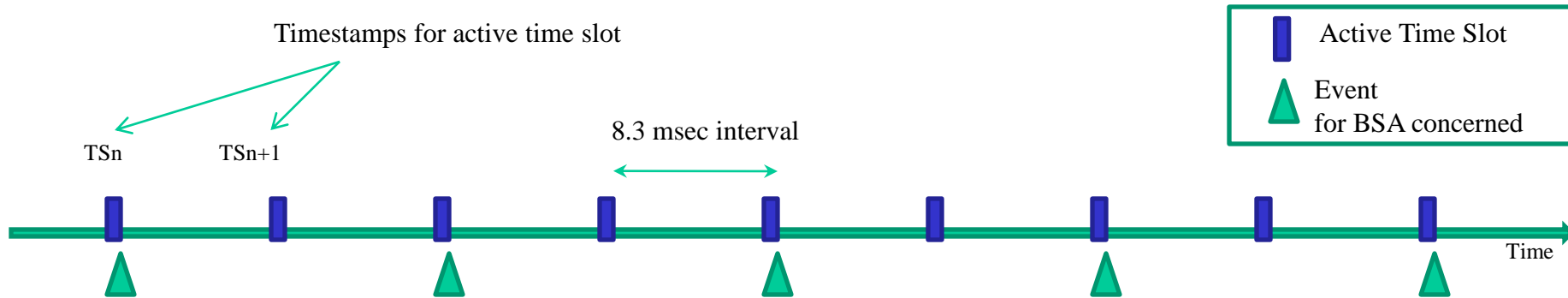
Success Scenario: if TSE=-2

- Device support provides timestamp TSn to the record instance
- Even, record processing is finished after TSn+1, the timestamp should be TSn.
- BSA is succeeded

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BSA aware timestamp and BSA fail/success scenario (4)

Timestamps for active time slot

| | Active Time Slot |
| Event for BSA concerned |

TSn   TSn+1

8.3 msec interval

Time

(1) Event system update internal timestamp tables with the given event number

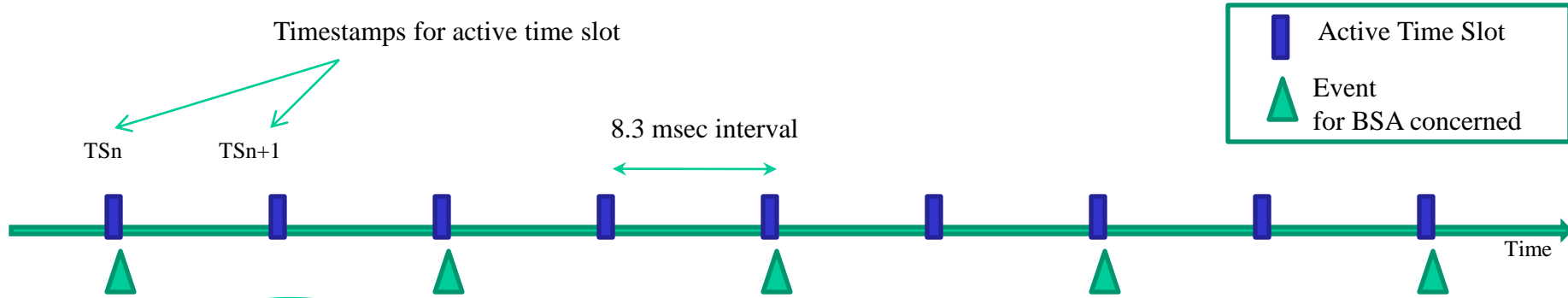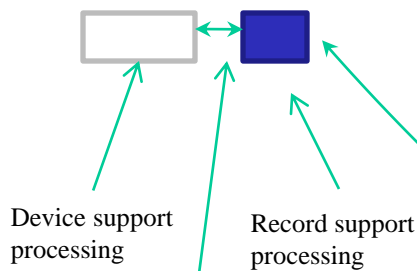| Event #	Description	Timestamp
0	Active timeslot	03/23/2011 14:30:11.1343234234
1	360Hz Fiducial	03/23/2011 14:30:11.12343443343
m		TSn

Device support processing

Record support processing

Undefined delay between Dev. and Rec.

(2) Record gets timestamp from the Event System Internal Table with the given event number

Success Scenario: if TSE=m (event for △

- Need to Enable VME IRQ for event m
- Event System maintain internal timestamp table for the events (including event m)
- Record gets latest timestamp from table for event number m

Controls

Guarantee that everything can be finished within 8.3 msec

LLRF PAD reading

HW Trigger

PAD

FNET

udpComm

DevPadDataProc

AI record

DOL

FLNK

AO in BSA

SCAN=I/O Intr
TSE=0, -1

Controls

BPM PAD reading

HW Trigger

PAD

FNET

udpComm

AI record

DOL

AO in BSA

FLNK

SCAN=I/O Intr
TSE=-2

Device support handles
Timestamp for data source PVs
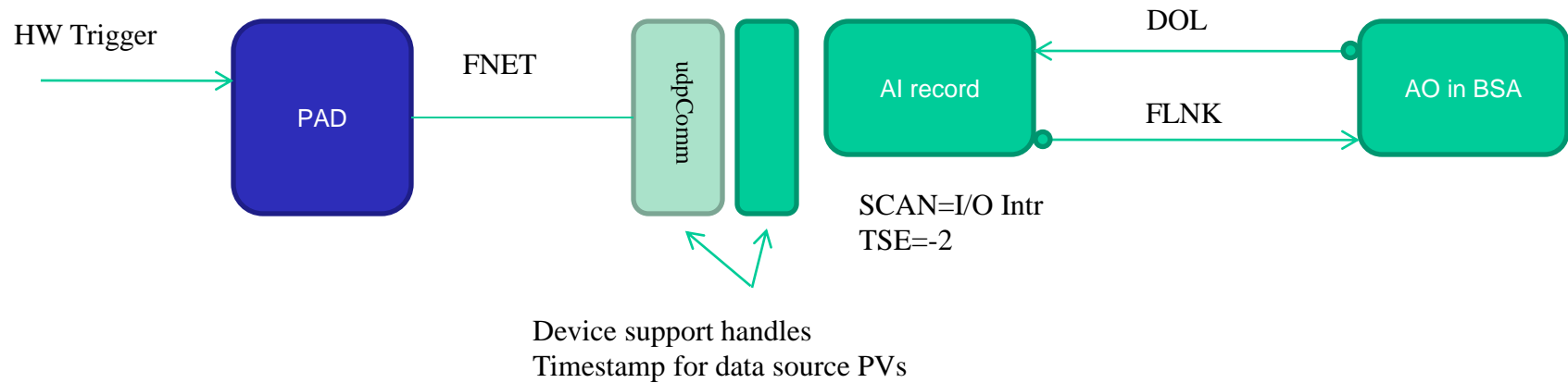
Example of Scenario (4): Long Processing Time

Record processing is spilled out to the next active time slot, but is not violated the dead-line for the next event.

HW Trigger with Event code n

Motor HW

AI record (Data Source)

DOL

FLNK

AO in BSA

SCAN=I/O Intr
TSE=n

Get timestamp from the latest event n, instead of the current active timeslot

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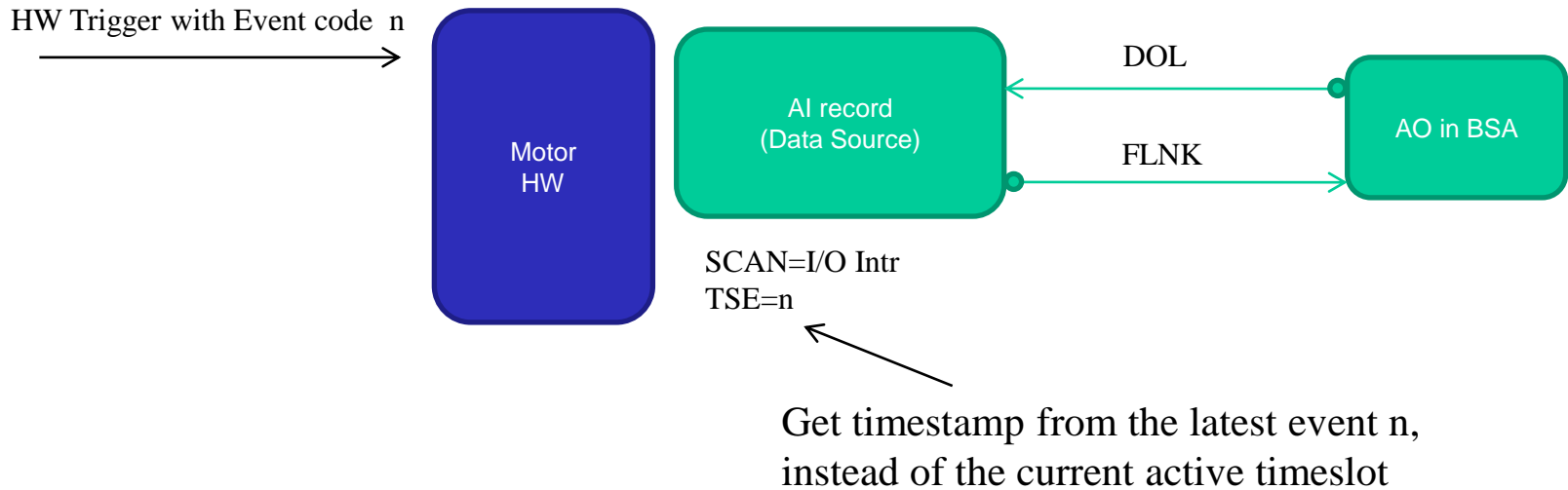
Example of Scenario (4) Asynchronous BSA?

No Sync with BSA

HW

Motor Record

INP

AI record
(Data Source)

DOL

AO in BSA

FLNK

SCAN=I/O Intr

SCAN=Event
EVENT=n
TSE=n

BSA Check Point AGAIN!

Data receptor

Device Support

Data Source PV

(*3)DOL

(*4)FLNK

AO in BSA

BSA Record

(*1) SCAN=I/O Intr? or EVENT?
(*2) TSE=0, -2

(*5)INP=@PV name for Data Source
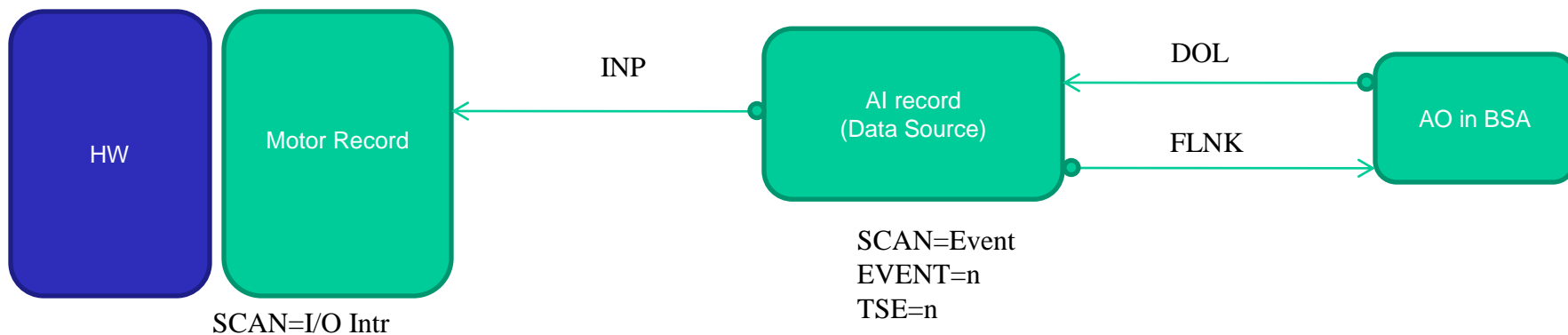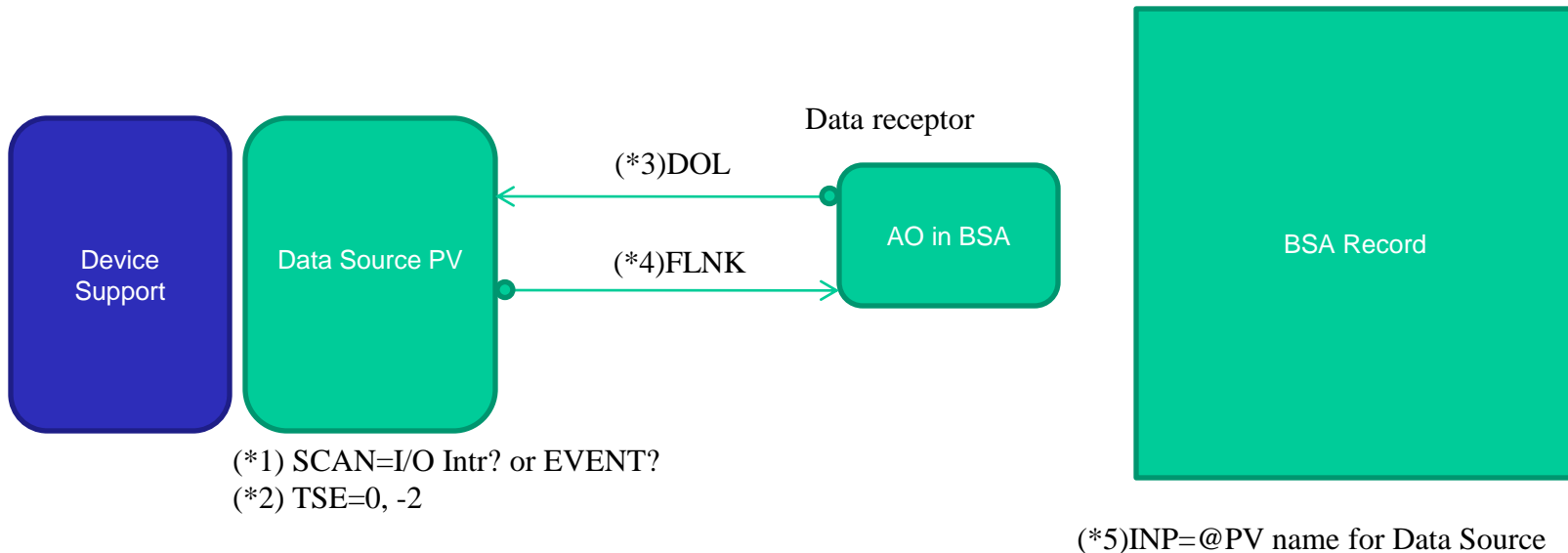
(*1) check up your data source driving mechanism
(*2) check up TSE in your data source, Please remind the success/fail scenario
(*3) (*5) check up if the PV name matched, DOL in data receptor and INP in BSA
(*4) check up the FLNK, your data source should drive the data receptor

SLAC
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